

PRODUCT SPECIFICATION

6162CIC

Bluetooth LE5.0 Module Datasheet

Version:v1.1

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

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6162CIC Module Datasheet

Ordering Information	Part NO.	Description
	FG6162CICX-02	6162CIC RTL8762CMF QFN40_5x5 On board PCB antennas,BT5.0+UART,Band RF output,PCB Version V2.0



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[illegible]

1. General Description

1.1 Introduction

Mesh self-organizing network type communication equipment, can efficiently and quickly form a non-central wireless broadband network; Supporting multi-hop relay can effectively expand the coverage radius of wireless network.

FN-link releases a low-cost, low-power Bluetooth 5.0 module with Mesh functionality. It is a highly integrated ARM Cortex-M4F 32-bit CPU, 160kByte RAM and 512kByte flash MCU, and Bluetooth 5.0 LE transceiver Mesh network solution.

The wireless module meets the Bluetooth 5.0 LE standard and provides UART interfaces for Bluetooth. Modules of moderate size, suitable for intelligent LED and other applications, can efficiently solve the complex environment such as high-rise, underground, tunnel, large complex emergency communication problems.

1.2 Description

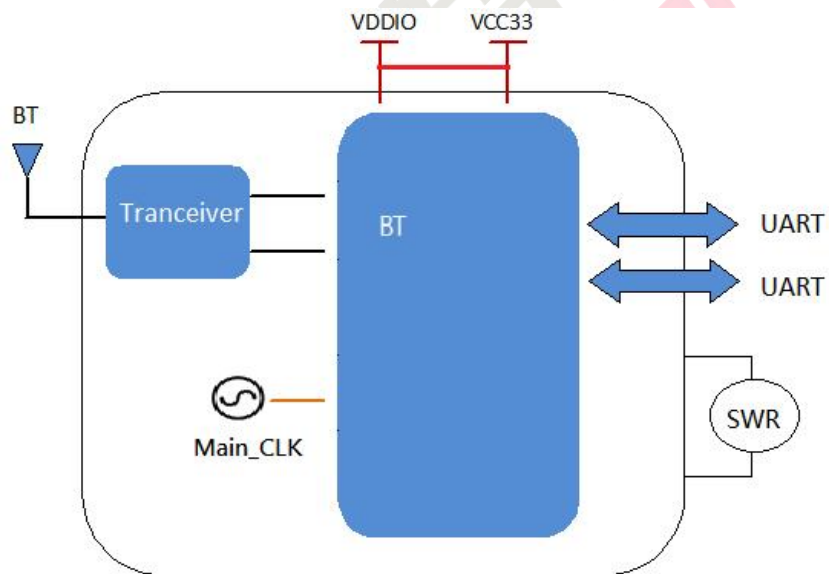
Model Name	6162CIC
Product Description	Support Bluetooth 5.0 functionalities
Dimension	L x W x T: 18.6X13X2.5 (typical) mm
BT Interface	UART
Operating temperature	-40° C to 85° C
Storage temperature	-40° C to 125° C

2. Features

General

- Supports Bluetooth 5 core specification
- Supports 2M LE , LE Long Range, LE Data Length Extensions (257 byte)
- Supports OTA (Over-the-Air)programming mechanism for firmware upgrade
- UART x 2, one for data transceiver, the other for firmware upgrade
- Embedded 4Mbits Flash
- Supports 5 GPIOs
- Embedded Switching Regulator(SWR) for low current consumption
- Package: 18.6X13X2.5mm

3. Block Diagram



4. General Specification

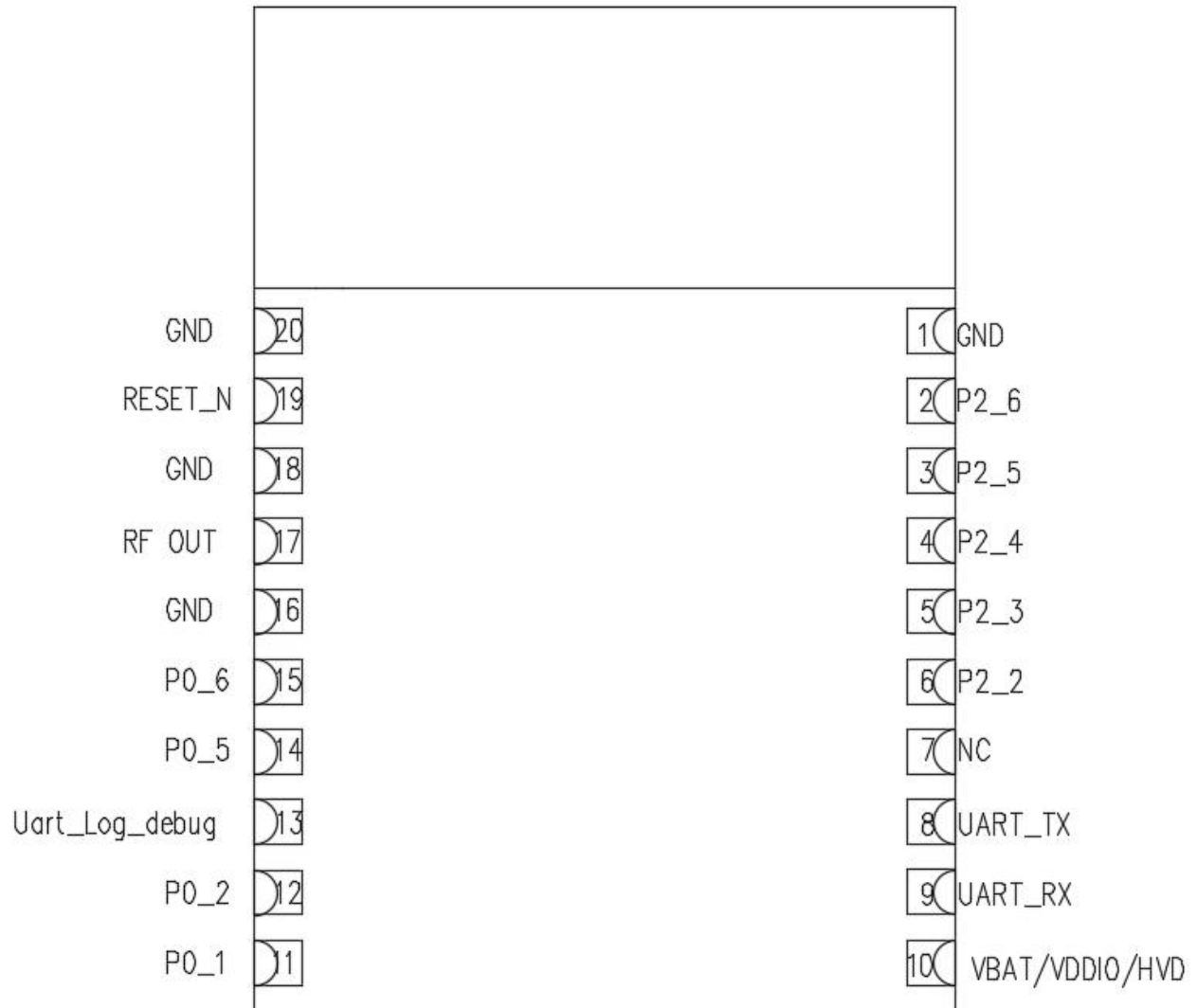
4.1 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.0 LE		
Host Interface	UART		
Antenna Reference	On board PCB antennas		
Frequency Band	2400 MHz ~ 2483.5 MHz		
Number of Channels	40（3 Advertising + 37 Data）		
Modulation	GFSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power	0	4	8
Sensitivity @ BLE=30.8%	-95		-90
Maximum Input Level	LE 1Mbps: -20dBm		

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	P	Ground connections	
2	P2_6	I/O	GPIO pin, refer to Pin Function Table Bluetooth UART interface_Data_Output	
3	P2_5	I/O	GPIO pin, refer to Pin Function Table Bluetooth UART interface_Data_Input	
4	P2_4	I/O	GPIO pin, refer to Pin Function Table Bluetooth Transceiver or Local Recognition 1:Bluetooth Transceiver 0:Local Recognition	
5	P2_3	I/O	GPIO pin, refer to Pin Function Table Bluetooth UART event wakeup	
6	P2_2	I/O	GPIO pin, refer to Pin Function Table	
7	NC1	—	No connect	
8	Uart_Tx	O	Software Upgrade UART interface_Data Output	
9	Uart_Rx	I	Software Upgrade UART interface_Data Input	
10	VBAT/VDDIO/HVD	P	I/O Voltage supply input 3.3V	
11	P0_1	I/O	GPIO pin, refer to Pin Function Table	
12	P0_2	I/O	GPIO pin, refer to Pin Function Table	
13	Uart_Log_debug	I/O	Log_Uart Interface_Data Output; Connect to GND for upgrade software (P0_3)	
14	P0_5	I/O	GPIO pin, refer to Pin Function Table	
15	P0_6	I/O	GPIO pin, refer to Pin Function Table	
16	GND	—	Ground connections	
17	RF OUT	NC1	RF OUT PIN (Alternative)	
18	GND	—	Ground connections	
19	Reset	I	Reset (Low active)	
20	GND	P	Ground connections	

P:POWER I:INPUT O:OUTPUT

Download; Test; AT command Default use pin 8, pin9

Before downloading, pull pin13 up before powering on the module

Function table:

RTL8752CMF RTL8762CMF	GPIO Index	ADC	Hardware Default Pull setting(100K) Reset state	Rom Code Setting	Pull resistor	Bootcode Default	Wakeup Function	Driver current	Power on trap	SPI 20MHz Timing Constrain PIN	IOB80 interface
P0_0	GPIO_0		Pull Down	Pull Down	10K/100K		Yes	8mA			
P0_1	GPIO_1		Pull Down	Pull Down	10K/100K		Yes	8mA			8080_D1
P0_2	GPIO_2		Pull Down	Pull Down	10K/100K		Yes	8mA			8080_D2
P0_3	GPIO_3		Pull Up	Output High	10K/100K	LOG_UART_TX	Yes	8mA	Power up latch internal pull high 1:Normal mode 0:Bypass mode		
P0_4	GPIO_4		Pull Down	Pull Down	10K/100K		Yes	8mA			8080_D1
P0_5	GPIO_5		Pull Down	Pull Down	10K/100K		Yes	8mA			8080_D3
P0_6	GPIO_6		Pull Down	Pull Down	10K/100K		Yes	8mA			
P0_7	GPIO_7		Pull Down	Pull Down	10K/100K		Yes	8mA			
P1_0	GPIO_8		Pull Up	Pull Up	10K/100K	SWDIO	Yes	8mA			
P1_1	GPIO_9		Pull Up	Pull Up	10K/100K	SWDCLK	Yes	8mA			
P1_2	GPIO_10		Pull Down	Pull Down	10K/100K		Yes	8mA			
P1_3	GPIO_11		Pull Down	Pull Up	10K/100K		Yes	8mA			8080_D2
P1_4	GPIO_12		Pull Down	Pull Up	10K/100K		Yes	8mA			8080_D3
P1_5	GPIO_13		Pull Down	Pull Down	10K/100K		Yes	8mA			
P1_6	GPIO_14		Pull Down	Pull Down	10K/100K		Yes	8mA			
P1_7	GPIO_15		Pull Down	Pull Down	10K/100K		Yes	8mA			
P8_0	GPIO_25		Pull Down	Pull Down	5K/50K		Yes	8mA			
32k_XI	GPIO_26		Pull Down	Pull Down	10K/100K		Yes	8mA			
32k_XO	GPIO_27		Pull Down	Output Low	10K/100K		Yes	8mA			
P2_0	GPIO_16	ADC/LPC(channel 0) Differential0	Pull Down	Pull Down	5K/50K		Yes	8mA			8080_RD#
P2_1	GPIO_17	ADC/LPC(channel 1) Differential0	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_2	GPIO_18	ADC/LPC(channel 2) Differential0	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_3	GPIO_19	ADC/LPC(channel 3) Differential1	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_4	GPIO_20	ADC/LPC(channel 4) Differential1	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_5	GPIO_21	ADC/LPC(channel 5) Differential1	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_6	GPIO_22	ADC(channel 6) Differential1	Pull Down	Pull Down	5K/50K		Yes	8mA			
P2_7	GPIO_23	ADC(channel 7) Differential1	Pull Down	Pull Down	5K/50K		Yes	8mA			
P3_0	GPIO_24		Pull Up	Pull Up	10K/100K	UART_TX	Yes	8mA			
P3_1	GPIO_25		Pull Up	Pull Up	10K/100K	UART_RX	Yes	8mA			
P3_2	GPIO_26		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI1_CLK	8080_RD#
P3_3	GPIO_27		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI1_MISO	8080_CS#
P3_4	GPIO_28		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI1_MOSI	8080_DCX
P3_5	GPIO_29		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI1_CSN	8080_WR#
P3_6	GPIO_30		Pull Down	Pull Down	10K/100K		Yes	8mA			8080_D0
P4_0	GPIO_28		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI0_CLK	8080_D4
P4_1	GPIO_29		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI0_MISO	8080_D5
P4_2	GPIO_30		Pull Down	Pull Down	10K/100K		Yes	8mA		SPI0_MOSI	8080_D6
P4_3	GPIO_31		Pull Up	Pull Up	10K/100K		Yes	8mA		SPI0_CSN	8080_D7

Pin Multiplexer:

All GPIO pins in the RTL8762C are configurable via the built-in pin multiplexer (PINMUX). Table 9 shows all GPIO pin configurations. Figure 13, page 25 shows the PINMUX and GPIO PADs control path. In the RTL8762C, all pins have an internal pull-up and pull-down resistor for controlling GPIO_PU and GPIO_PD.

Table 9. Pin Multiplexer (PINMUX)

0	IDEL	25	qdec_phase_a_z	50	SPI0_CLK (master only)	75	KEY_COL_17	100	Reserved	125	Reserved
1	HCI_UART_TX	26	qdec_phase_b_z	51	SPI0_M0 (master only)	76	KEY_COL_18	101	Reserved	126	Reserved
2	HCI_UART_RX	27	UART2_TX	52	SPI0_M1 (master only)	77	KEY_COL_19	102	PDM (clk)	127	MCLK
3	HCI_UART_CTS	28	UART2_RX	53	SPI2W_DATA (master only)	78	KEY_ROW_0	103	PDM (data)		
4	HCI_UART_RTS	29	UART1_TX	54	SPI2W_CLK (master only)	79	KEY_ROW_1	104	UART2_CTS		
5	I2C0_CLK	30	UART1_RX	55	SPI2W_CS (master only)	80	KEY_ROW_2	105	UART2_RTS		
6	I2C0_DAT	31	UART1_CTS	56	SWD_CLK	81	KEY_ROW_3	106	Reserved		
7	I2C1_CLK	32	UART1_RTS	57	SWD_DIO	82	KEY_ROW_4	107	Reserved		
8	I2C1_DAT	33	IRDA_TX	58	KEY_COL_0	83	KEY_ROW_5	108	Reserved		
9	PWM2_P	34	IRDA_RX	59	KEY_COL_1	84	KEY_ROW_6	109	Reserved		
10	PWM2_N	35	UART0_TX	60	KEY_COL_2	85	KEY_ROW_7	110	Reserved		
11	PWM3_P	36	UART0_RX	61	KEY_COL_3	86	KEY_ROW_8	111	Reserved		
12	PWM3_N	37	UART0_CTS	62	KEY_COL_4	87	KEY_ROW_9	112	Reserved		
13	PWM0	38	UART0_RTS	63	KEY_COL_5	88	KEY_ROW_10	113	Reserved		
14	PWM1	39	SPI1_SS_N_0 (master only)	64	KEY_COL_6	89	KEY_ROW_11	114	Reserved		
15	PWM2	40	SPI1_SS_N_1 (master only)	65	KEY_COL_7	90	DWGPIO	115	Reserved		
16	PWM3	41	SPI1_SS_N_2 (master only)	66	KEY_COL_8	91	I2S_LRCLK	116	Reserved		
17	PWM4	42	SPI1_CLK (master only)	67	KEY_COL_9	92	I2S_BCLK	117	EN_EXPA		
18	PWM5	43	SPI1_M0 (master only)	68	KEY_COL_10	93	I2S_ADCCDAT	118	EN_EXLNA		
19	PWM6	44	SPI1_M1 (master only)	69	KEY_COL_11	94	I2S_DACDAT	119	ANT_SW0		
20	PWM7	45	SPI0_SS_N_0 (slave)	70	KEY_COL_12	95	Reserved	120	ANT_SW1		
21	qdec_phase_a_x	46	SPI0_CLK (slave)	71	KEY_COL_13	96	DMIC1_CLK	121	ANT_SW2		
22	qdec_phase_b_x	47	SPI0_SO (slave)	72	KEY_COL_14	97	DMIC1_DAT	122	ANT_SW3		
23	qdec_phase_a_y	48	SPI0_SI (slave)	73	KEY_COL_15	98	Reserved	123	Reserved		
24	qdec_phase_b_y	49	SPI0_SS_N_0 (master only)	74	KEY_COL_16	99	Reserved	124	Reserved		

6. Electrical Specifications

6.1 Power Supply DC Characteristics

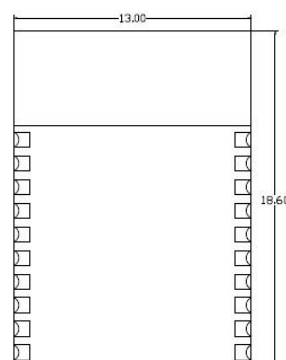
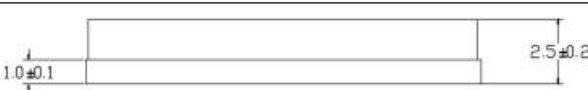
	MIN	TYP	MAX	Unit
Operating Temperature	-40	25	80	deg.C
VBAT&VDDIO	2.7	3.0	3.6	V

6.2 Power Consumption

Power Consumption		VCC33 = 3.0V(Unit:mA)
	BT on	11.3

7. Size reference

7.1 Module Picture

L x W : 18.6 x 13 (±0.2) mm	
H: 2.5 (±0.2) mm	
Weight	0.8g(±0.1)g

The physical picture will be updated in a later version

7.2 List of certified information

Certification project	Certificate number
SRRC	CMIIT ID:24J43T23H406
FCC	2AATL-6162CIC
CE	0370-RED-7875
IC	12425A-6162CIC
NCC	TBD
KCC	TBD
TELEC	TBD
Brazil	TBD
Argentina	TBD
Japan	TBD

7.3 Marking Description



备注:

二维码内容: 112233445566;6162CIC;234502

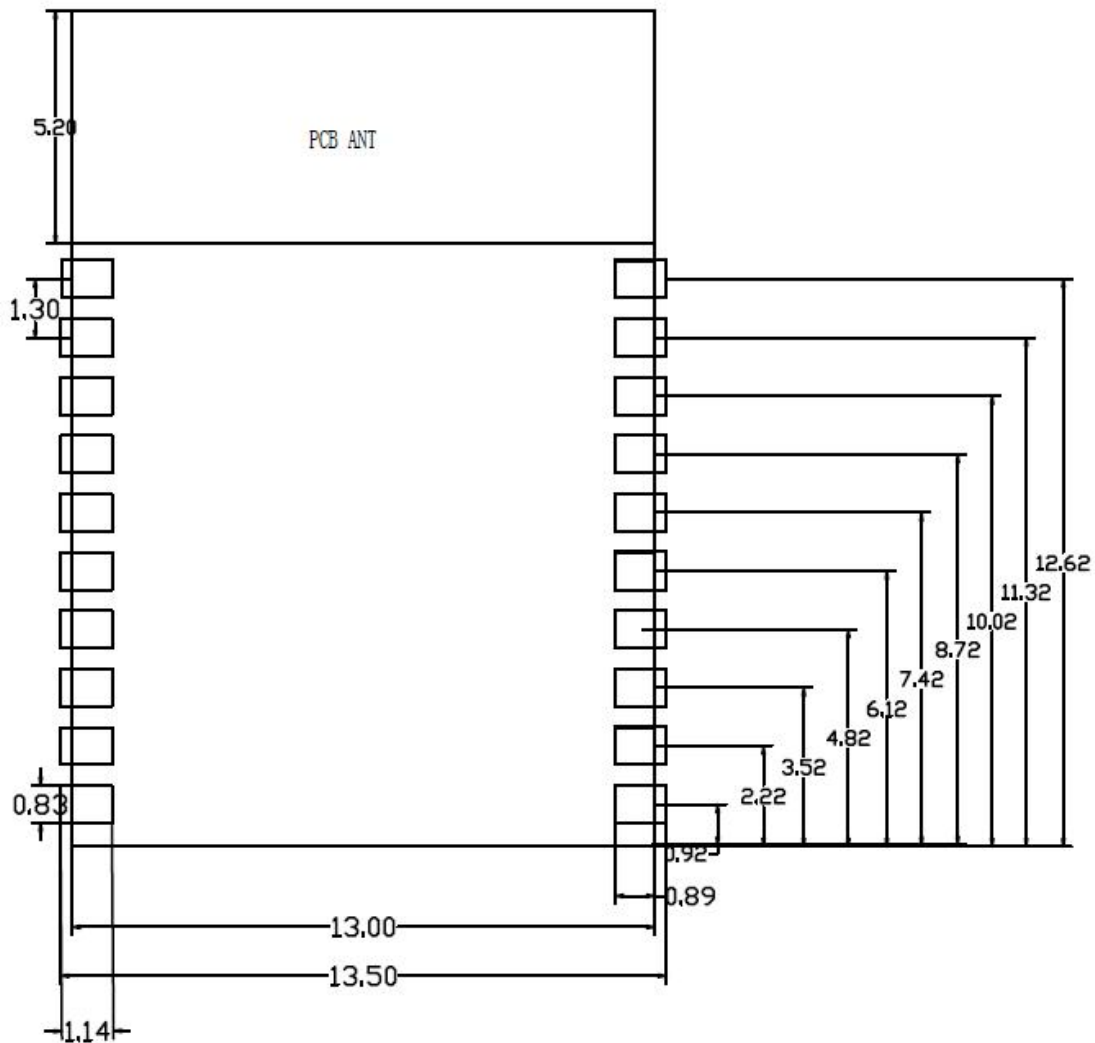
1. Fn-Link 商标 LOGO

2. 机型: 6162CIC

3. 二维码: 编码规则为 “ble 地址; 机型名称; datecode+成品料号后缀”

例如: 112233445566;6162CIC;234502 (MAC 地址以实际为准, 2345 为生产周期, 23 年 45 周, 02 为成品料号后缀)

7.4 Layout Recommendation

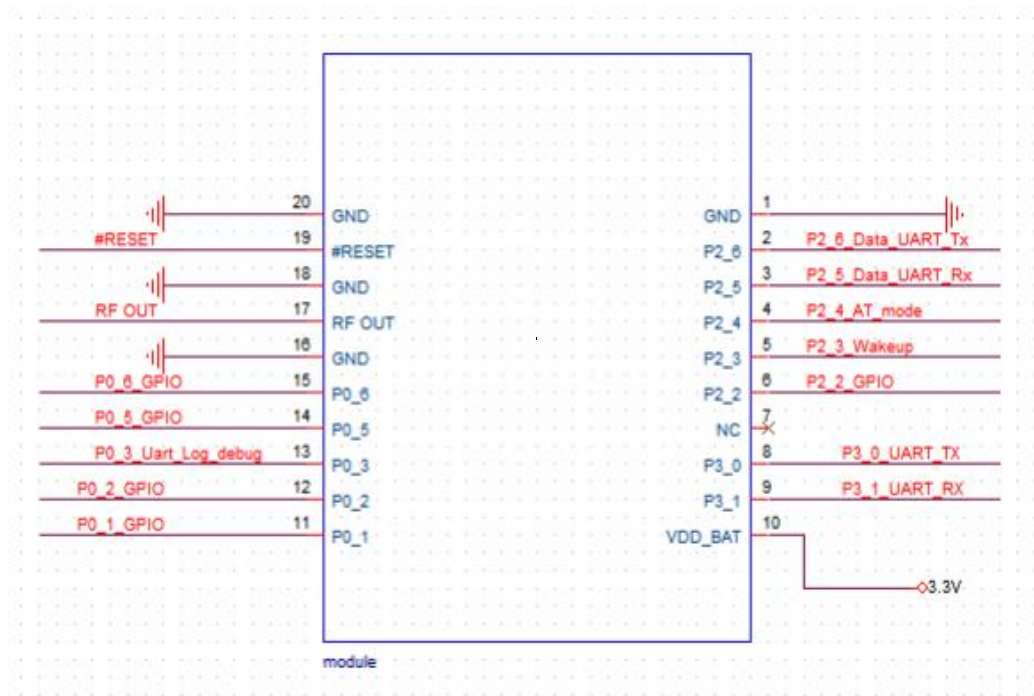


8. The Key Material List

Item	Part Name	Description	Manufacturer
1	Crystal	3225 40MHz 9pF +/-10PPM	ECEC, TKD, Hosonic, JWT, TXC
2	Chipset	RTL8762CMF-CG QFN40	Realtek

3	PCB	6162CIC green,2L,13×18.6×1.0mm	XY-PCB, GDKX, Sunlord, SLPCB
4	Shielding	6162CIC shielding	信太, 精力通

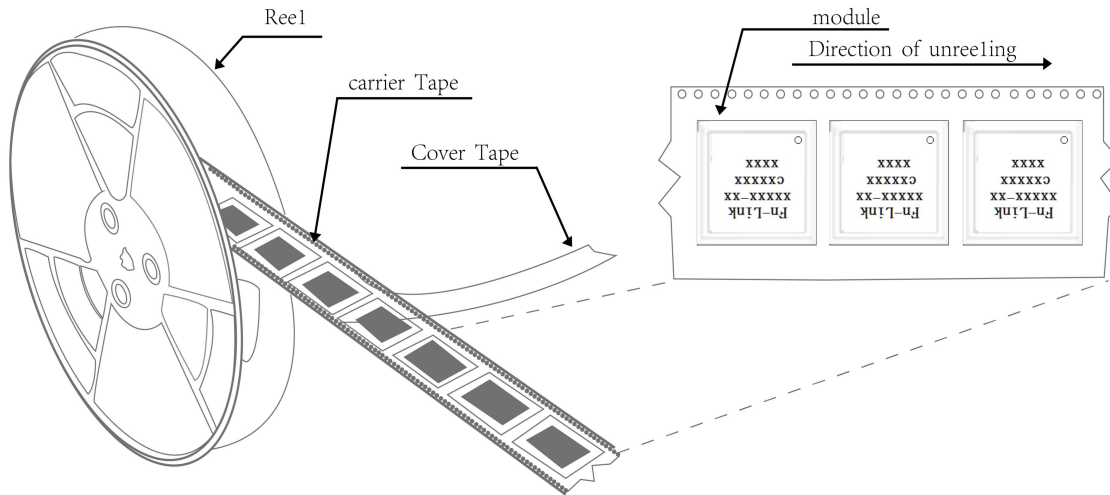
9. Reference Design



10. Package

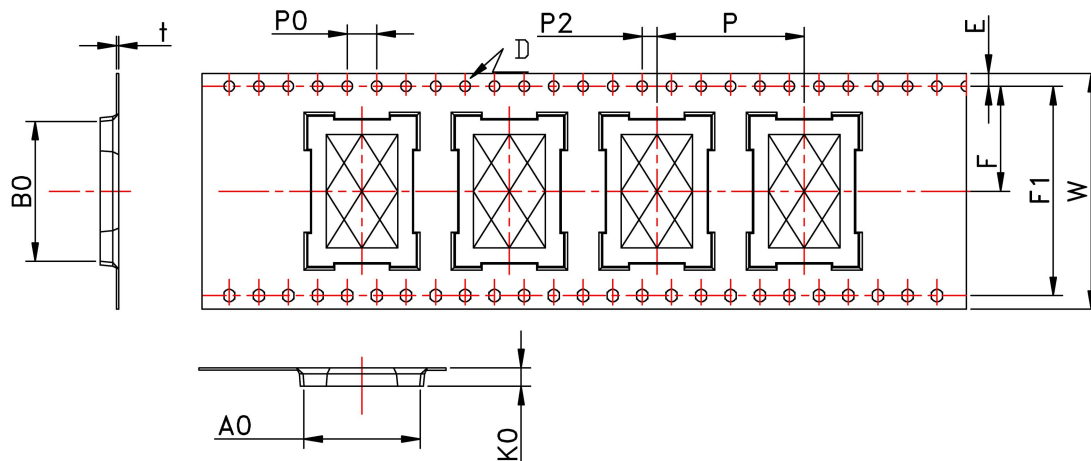
10.1 Reel

A roll of 1000pcs



10.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	32	13.30	19.00	1.5	1.75	14.20	28.4	2.80	4.0	2.0	20.0	0.30
TOLE	$\begin{smallmatrix} +0.3 \\ -0.3 \end{smallmatrix}$	± 0.18	± 0.18	$\begin{smallmatrix} +0.1 \\ -0.0 \end{smallmatrix}$	± 0.1	± 0.15	± 0.10	± 0.10	± 0.1	± 0.15	± 0.1	± 0.05



10.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 32mm*32.6m the cover tape :25.5mm*32.6m

Color of plastic disc: blue



NY bag size:450X415mm



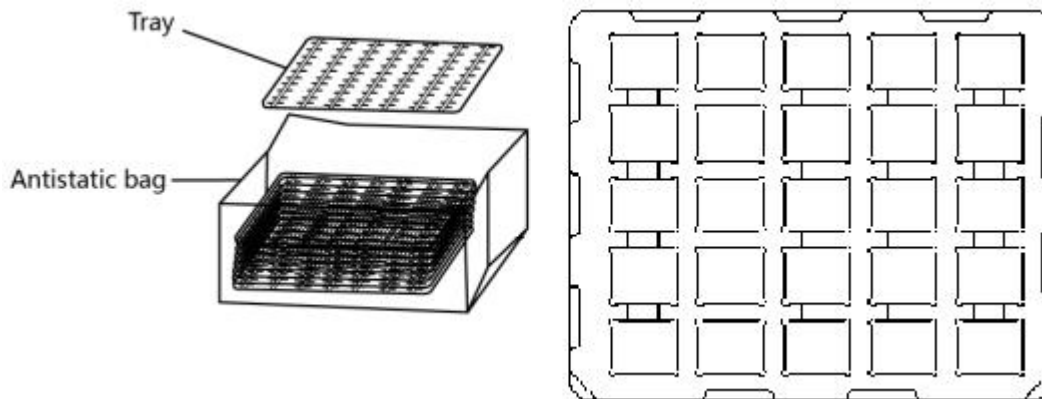
size : 350*350*35mm



The packing case size:360X210X370mm

10.4 Tray

Use pallet packaging for less than 300 pieces



11. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- d) Baking is required if conditions b) or c) are not respected
- e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more