6189N-SFC

Wi-Fi Single-band 1X1 802.11b/g/n

Module Datasheet

Proprietary & Confidential Information

6189N-SFC Module Datasheet

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Customer Approval : _____ Company

_____ Title

_____ Signature

_____ Date

_____ Fn-Link

Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2021/04/22	New version	Lxy	Szs
1.1	2021/6/10	Added antenna clearance description	Lxy	Lgp
1.2	2023/08/17	Update Recommended Reflow Profile	Lxp	Lxy
1.3	2023/10/26	Update Host Interface Timing Diagram	Lxp	Lxy
1.4	2023/11/28	Add Certificate No	LXP	LXY
1.5	2024/10/15	Add ESD Manufacturer	LXP	LXY

CONTENTS

1 Overview

1.1 Introduction

6189N-SFC is a highly integrated and excellent performance Wireless LAN (WLAN) SDIO network interface device. High-speed wireless connection up to 150 Mbps. It can be easily manufactured on SMT process.

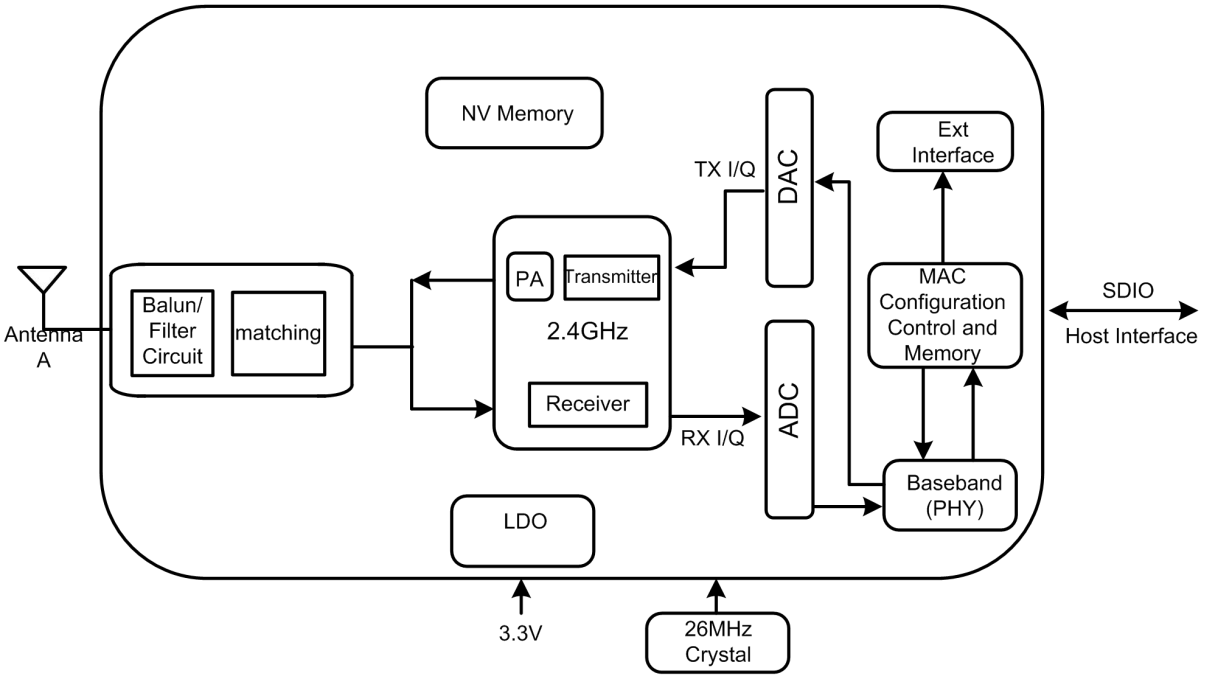
This WLAN Module design is based on Realtek RTL8189FTV-VC-CG. It is a highly integrated single-chip Wireless LAN (WLAN) SDIO network interface controller complying with the 802.11n specification. It combines a MAC, a 1T1R capable baseband, and RF in a single chip. It is designed to provide excellent performance with low power Consumption and enhance the advantages of robust system and cost-effective.

This compact module is a total solution for Wi-Fi technology. The module is specifically developed for Smart phones and Portable devices.

1.2 Features

- Operate at ISM frequency bands (2.4GHz)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

Block Diagram:



1.3 General Specification

Model Name	6189N-SFC
Product Description	Support Wi-Fi functionalities
Dimension	L x W x T: 23 x 21 x 4.8 (typical) mm
Wi-Fi Interface	Support SDIO
Operating temperature	0°C to 70°C
Storage temperature	-55°C to +125°C

1.4 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	0	25	70	deg.C
VBAT	3.0	3.3	3.6	V
VDDIO	1.7	1.8 or 3.3	3.6	V

※1.5 EEPROM Information

WI-FI

Vendor ID	024C
Product ID	F179

2 General Specification

2.1 Wi-Fi RF Specifications

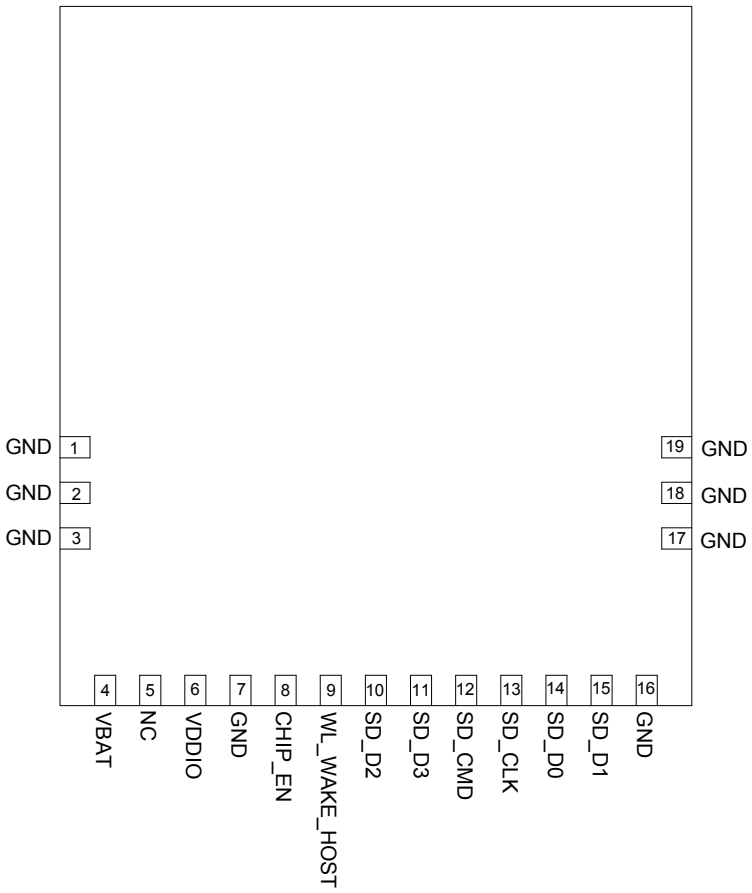
Features	Descriptions
Main Chipset	Realtek RTL8189FTV-VC-CG
Operating Frequency	2.400～2.4835GHz
Operating Voltage	3.3Vdc ±10% I/O supply voltage
Host Interface	SDIO/GSPI
WIFI Standard	Wi-Fi: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n,
Modulation	Wi-Fi: 802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps), BPSK(1Mbps), 802.11 g/n: OFDM

PHY Data rates	Wi-Fi: 802.11b: 11, 5.5, 2, 1 Mbps 802.11g: 54, 48, 36, 24, 18, 12, 9, 6 Mbps 802.11n: up to 150Mbps
Transmit Output Power	Wi-Fi: 802.11b@11Mbps 16±2dBm 802.11g@54Mbps 14±2dBm 802.11n@65Mbps 13±2dBm Other rate power control by power by rate.
EVM	802.11b /11Mbps: EVM≦-9dB 802.11g /54Mbps: EVM≦-25dB 802.11n /65Mbps: EVM≦-28dB
Receiver Sensitivity (HT20)	802.11b@8% PER 11Mbps< -82dBm
	802.11g@10% PER 54Mbps< -71dBm
	802.11n@10% PER MCS 7 <-67dBm
Operating Channel	Wi-Fi 2.4GHz: 11: (Ch. 1-11) – United States(North America) 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan
Media Access Control	Wi-Fi: CSMA/CA with ACK
Network Architecture	Wi-Fi: Ad-hoc mode (Peer-to-Peer) Infrastructure mode Software AP Wi-Fi Direct
Security	Wi-Fi: WPA, WPA-PSK, WPA2, WPA2-PSK, WEP 64bit & 128bit,
Antenna	On Board antenna
OS Supported	Android /Linux/ Win CE /iOS /XP/WIN7
Dimension	Typical L x W x H 23x21x4.8mm

3 Pin Assignments

3.1 Pin Outline

<TOP>



3.2 Pin Definition

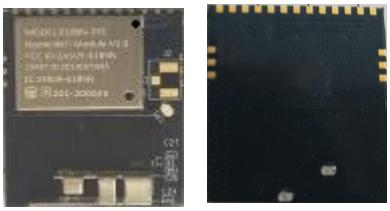
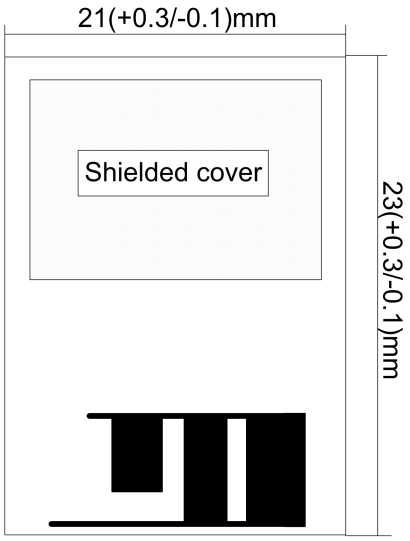
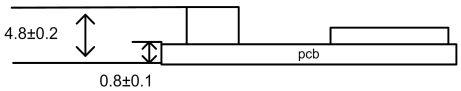
NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	GND		Ground connections	
3	GND		Ground connections	
4	VBAT	P	Supply 3.3V	3.3V
5	NC		Floating (Don’t connected to ground)	
6	VDDIO	P	I/O Voltage supply input 1.8V to	1.8V ~ 3.3V

			3.3V	
7	GND		Ground connections	
8	CHIP_EN	I	Wi-Fi enable pin, default pull high	3.3V
9	WL_WAKE_HOST	I/O	WLAN to wake-up HOST	1.8V ~ 3.3V
10	SD_D2	I/O	SDIO Data line 2	1.8V ~ 3.3V
11	SD_D3	I/O	SDIO Data line 3	1.8V ~ 3.3V
12	SD_CMD	I/O	SDIO Command Input	1.8V ~ 3.3V
13	SD_CLK	I	SDIO Clock Input	1.8V ~ 3.3V
14	SD_D0	I/O	SDIO Data line 0	1.8V ~ 3.3V
15	SD_D1	I/O	SDIO Data line 1	1.8V ~ 3.3V
16	GND		Ground connections	
17	GND		Ground connections	
18	GND		Ground connections	
19	GND		Ground connections	

P:POWER I:INPUT O:OUTPUT

4 Dimensions

4.1 Module Picture

<table>
<tr><td>L x W : 23 x 21 (+0.3/-0.1) mm
  </td><td> 
</td></tr>
<tr><td>H: 4.8 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>1.65g</td></tr>
</table>

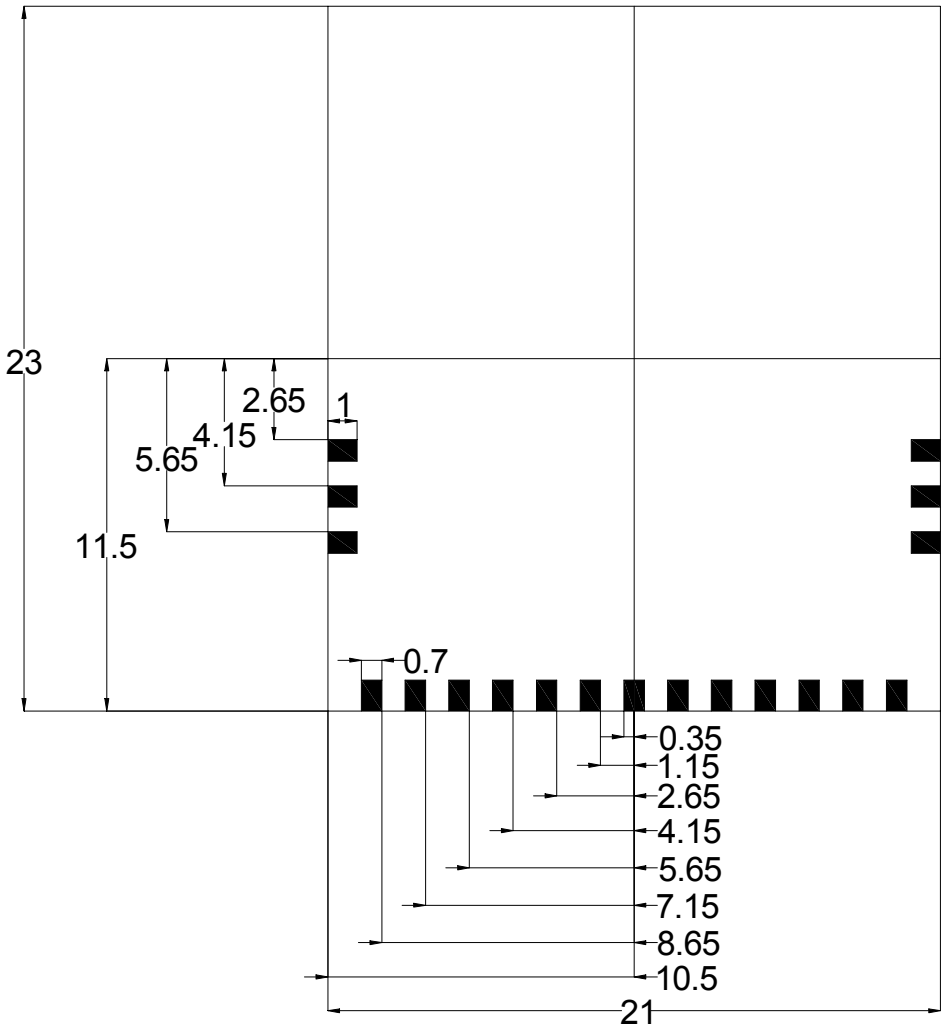
4.2 Marking Description

打黑点标识-03 机型

4.3 List of certified information

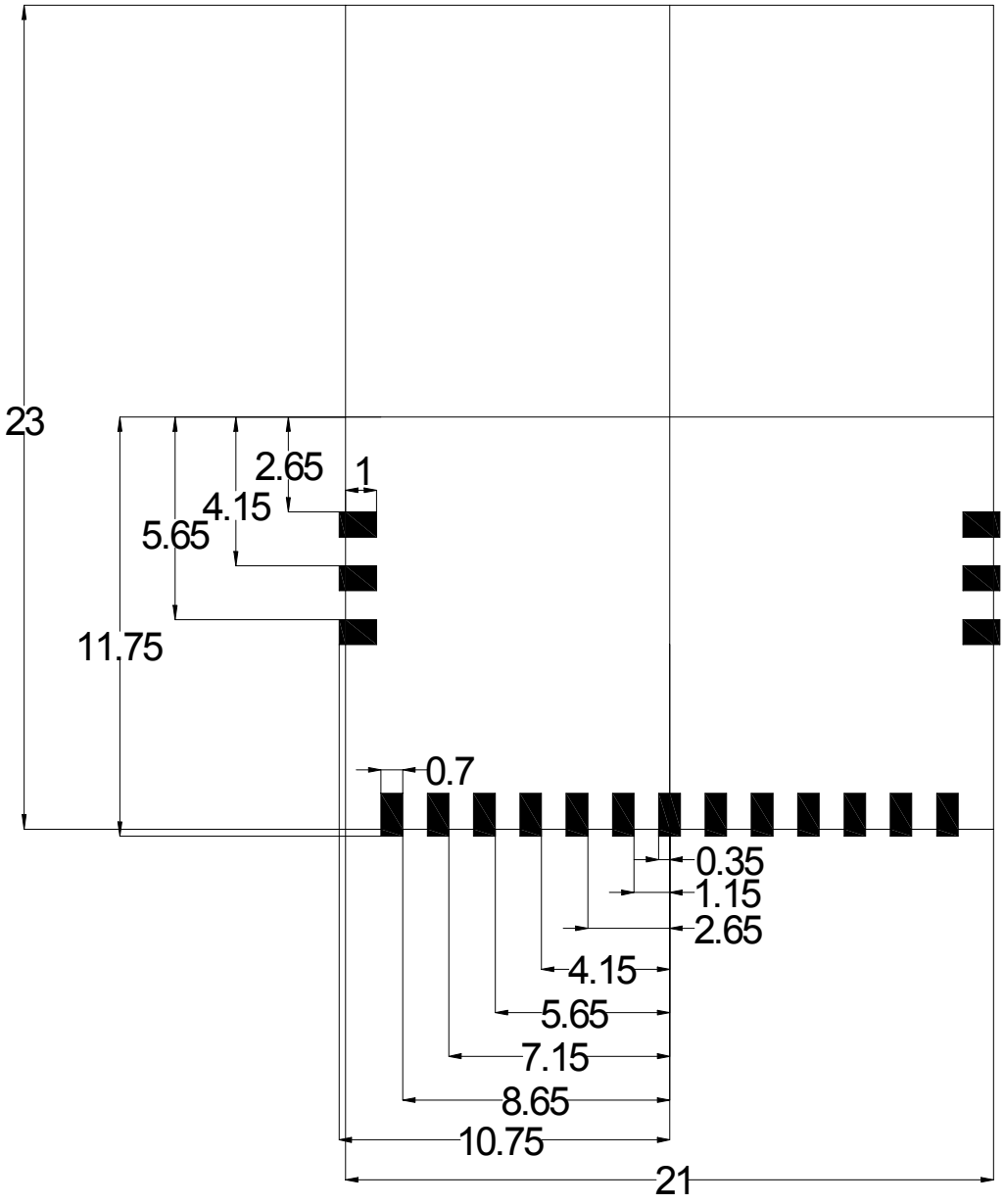
Certification project	Certificate number
SRRC	TBD
FCC	2AATL-6189N-SFC
CE	TCF-983CC20
IC	24844- 6189NSFC
NCC	CCAP23Y10050T0
KCC	R-R-FNL-6189N-SFC
TELEC	214-125865
Brazil	TBD
Argentina	TBD
Japan	TBD

4.4 Module Physical Dimensions



4.5 Layout Reference

(unit: mm)



6 Host Interface Timing Diagram

6.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR12(25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO

pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

6.2 SDIO interface Timing Diagram

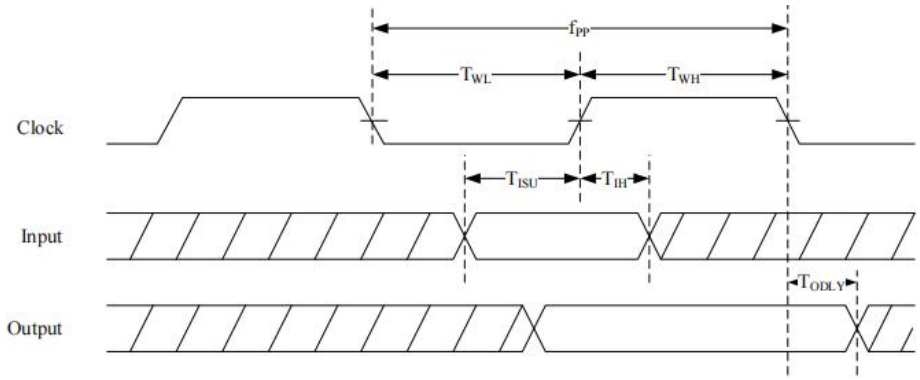


Figure 3. SDIO Interface Timing

Table 10 SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns

		HS	7		
T_{ISU}	Input setup time	DEF	5		ns
		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

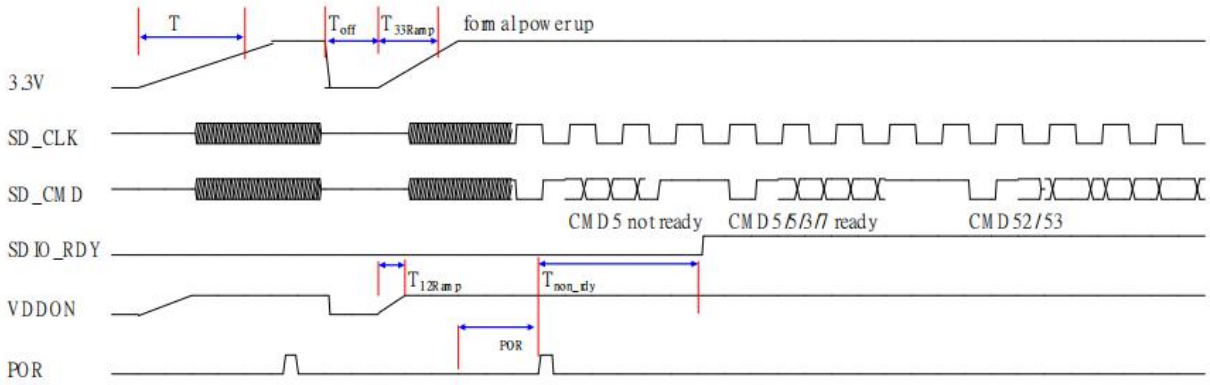
■ SDIO Interface Signal Level

The SDIO signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8189FTV-VQ1 SDIO interface via VDIO_SDIO pin (pin19).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.2.2.

6.3 SDIO Power-on sequence

After power on, the SDIO interface is selected by RTL8189FTV-VQ1 automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended:



Variable definition:

T33ramp': The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

Toff : The duration the 3.3V is cut off before formal power up.

T33ramp: The 3.3V main power ramp up duration

T12ramp: The internal 1.2V ramp up duration.

T_{POR}: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T_{non_rdy}: SDIO not ready duration, in this state, RTL8723AS may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuits during T_{non_rdy} duration. After autoload done, the SDIO responds command with ready bit set. After CMD5/ 5/ 3/ 7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

The typical timing spec is shown as follows:

Table 11 SDIO Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	0.2	0.5	2.5	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

6.4 Power off by chip_en sequence

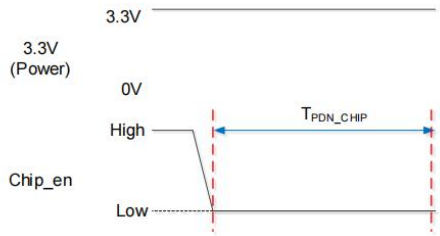


Figure 4. Power Off by chip_en Sequence

Table 12. Power Off by WL# and BT_DIS# Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PDN_CHIP}	10	100	--	ms	Chip_en keep low duration

Chip_en can externally shutdown the RTL8189FTV –VQ1 when chip_en is pulled low. The keeping low duration must be more than T_{PDN_CHIP}

6.5 Power off by 3.3V power sequence

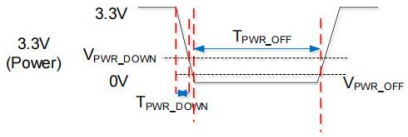


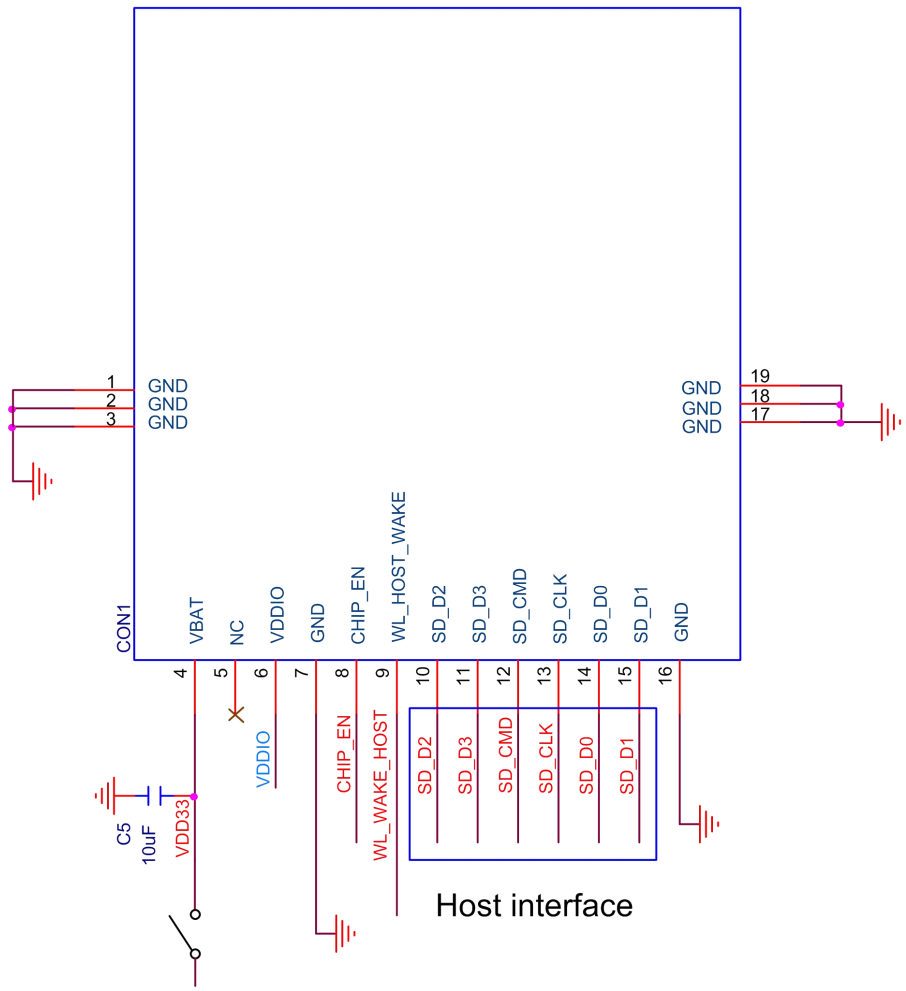
Figure 5. Power Off by 3.3V power Sequence

Table 13. Power Off by 3.3V power Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PWR_OFF}	10	100	--	ms	3.3V power off time
V_{PWR_OFF}	--	--	0.4	V	3.3V power off voltage
V_{PWR_DOWN}	--	--	0.7	V	3.3V power down voltage
T_{PWR_DOWN}	--	--	10	ms	3.3V power down time

When 3.3V power off and on afterward, the voltage of 3.3V power must keep lower than V_{PWR_OFF}, and the 3.3V power keeping off duration must be more than T_{PWR_OFF}

7 Reference Design

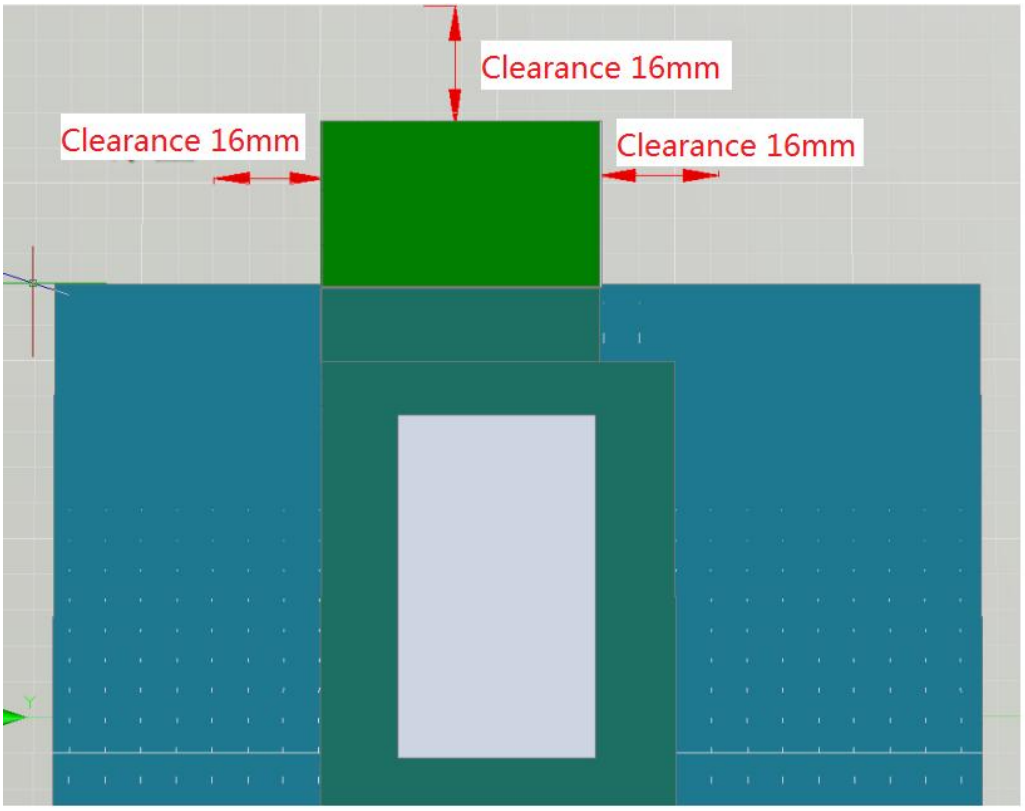


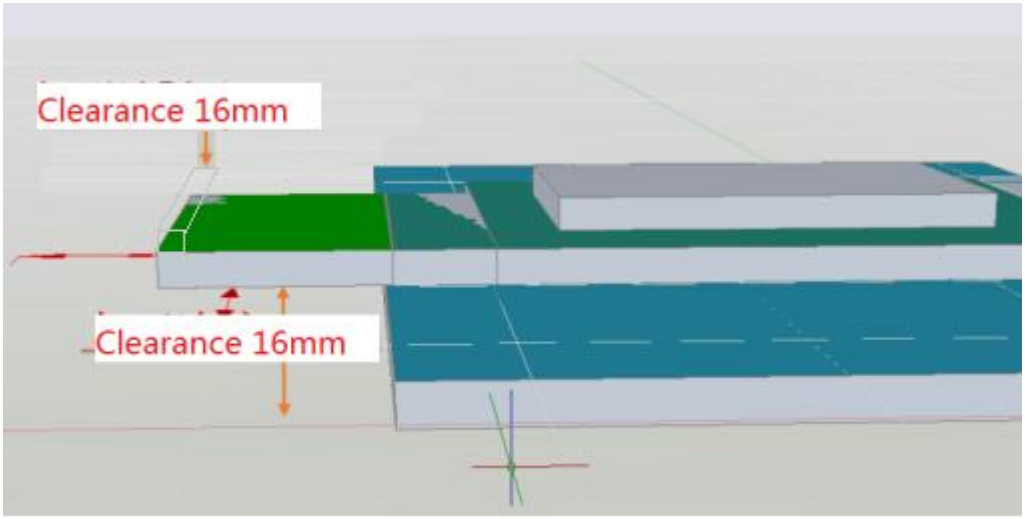
Note:

1. chip_EN could not use for module power off, please switch the 3.3V power for module on/off.

2.please keep the antenna on no metal area. Keep clearance as below shown.

3. 天线性能务必在整机安装后进行暗室测试确认。


Clearance 16mm
Clearance 16mm
Clearance 16mm


Clearance 16mm
Clearance 16mm

8 Ordering Information

Part No.	Description
FG6189NSFC-03	RTL8189FTV-VC-CG b/g/n, Wi-Fi, 1T1R, 23X21mm, SDIO, PCB V3.0 with antenna

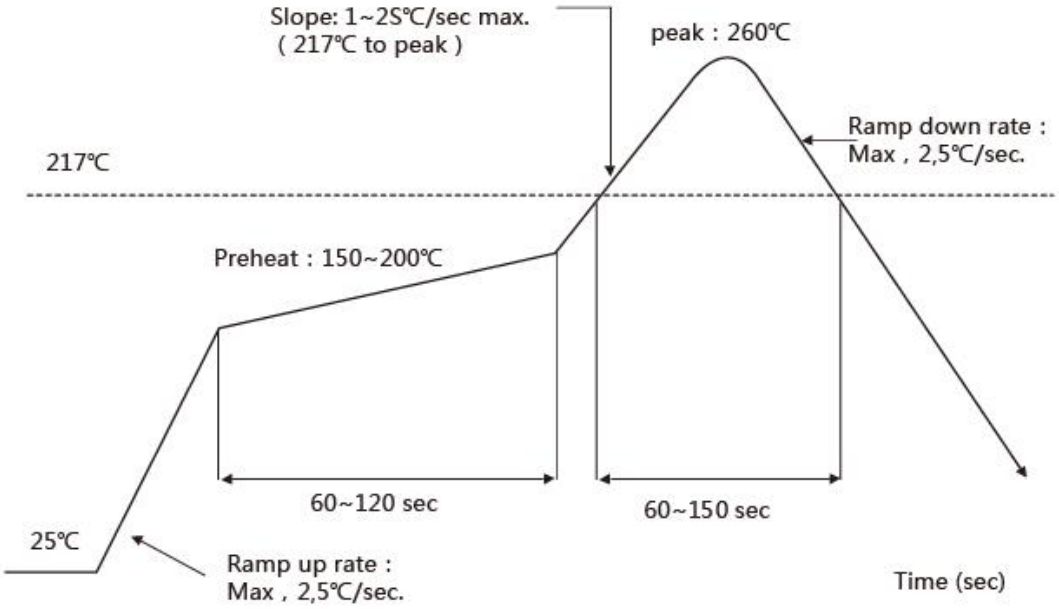
9 The Key Material List

Shielding cover	6189N-SFC V1.0 Shielding cover,height=1.4 mm	suntech，Jlitong
Crystal	26mhz 3225 ±10ppm, 10.5pF	HOSONIC,ECEC,TKD,JWT
ESD	0402 5.5V 0.1pF	Sunlord,Murata,Wayon,
Chipset	RTL8189FTV-VC-CG	Realtek
PCB	6189N-SFC V3.0 black，23x21-0.8mm	XY-pcb,Sunlord,KX-pcb,SL-PCB

10 Environmental Requirements

10.1 Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak Temperature : <260°C
Number of Times : ≤2 times



10.2 Patch Wi-Fi modules installed before the notice

Wi-Fi module installed note:

1. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil.
2. Take and use the WIFI module, please insure the electrostatic protective measures.
3. Reflow soldering temperature should be according to the customer the main size of the products, such as the temperature set at 250 + 5 ℃ for the MID motherboard.

About the module packaging, storage and use of matters needing attention are as follows:

1. The module of the reel and storage life of vacuum packing: 1). Shelf life: 8 months, storage environment conditions: temperature in: < 40 ℃, relative humidity: < 90% r.h.
2. The module vacuum packing once opened, time limit of the assembly:

Card:1) check the humidity display value should be less than 30% (in blue), such as: 30% ~ 40% (pink), or greater than 40% (red) the module have been moisture absorption.

2.) factory environmental temperature humidity control: ≦ -30 ℃, ≦ 60% r.h..

3). Once opened, the workshop the preservation of life for 168 hours.

3. Once opened, such as when not used up within 168 hours:

1). The module must be again to remove the module moisture absorption.

2). The baking temperature: 125 ℃, 8 hours.

3). After baking, put the right amount of desiccant to seal packages.

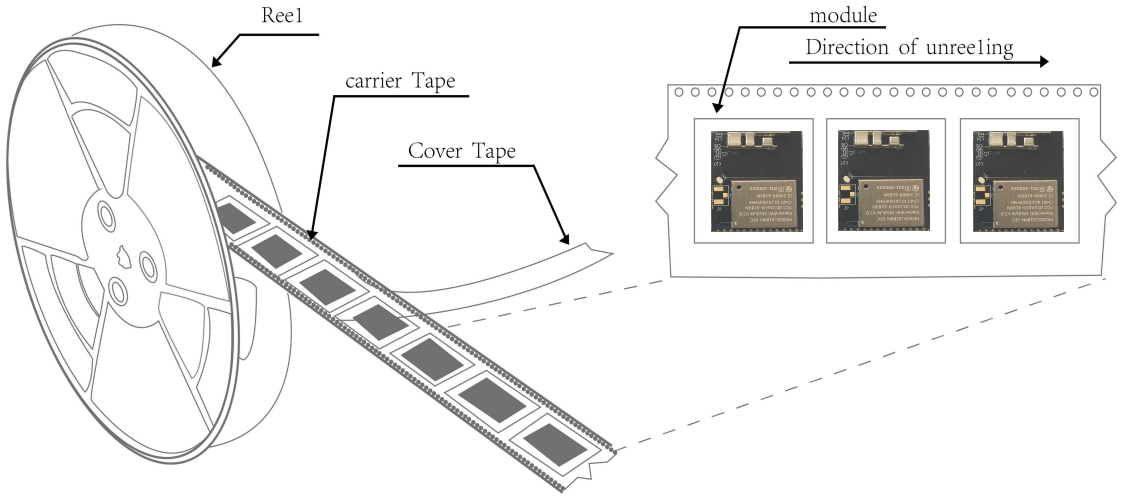
10.3 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:
a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity(RH).
b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

11 Package

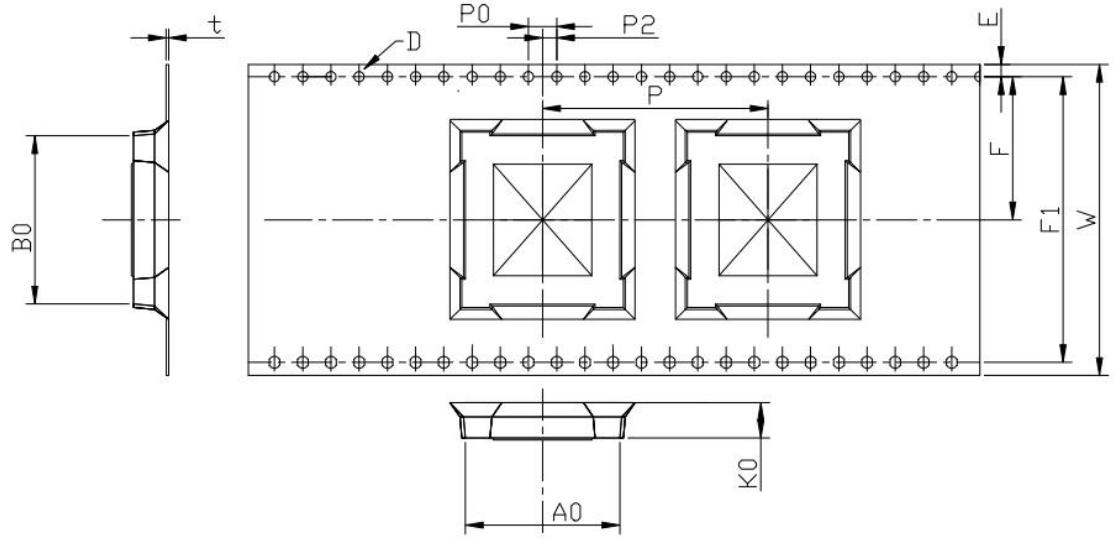
11.1 Reel

A roll of 350pcs



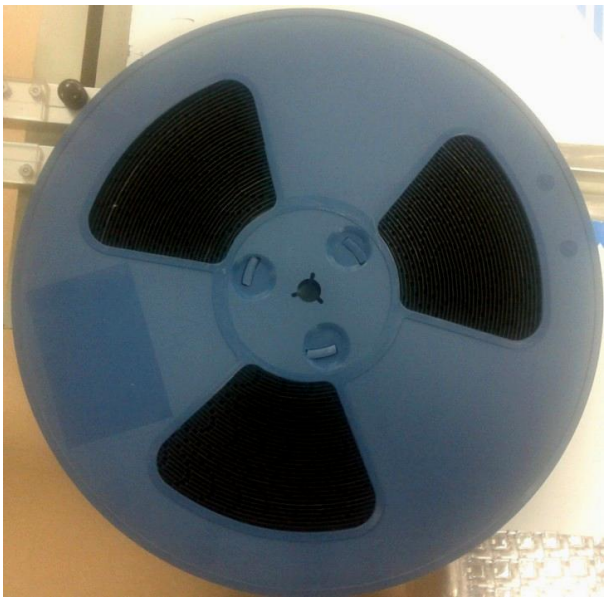
11.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	44	21.75	23.75	1.5	1.75	20.2	40.4	5.00	4.0	2.0	32.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05



11.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape:44mm*12.48m the cover tape :37.5mm*12.48m

Color of plastic disc:blue

A roll of 350pcs

NY bag size:420mm*450mm

size ： 335*335*55mm

The packing case size:335*255*370mm

11.4 Tray

Use pallet packaging for less than 300 pieces